What is claimed is:

1. A structure for a wafer level packaging, comprising :

pluralities of dies are adjoining each other, each of said pluralities of dies having a photosensitive zone;

pluralities of spacer walls are placed on the pluralities of dies, wherein each of said photosensitive zone is placed between said pluralities of spacer walls;

pluralities of sealant are placed on the pluralities of dies, wherein each of said pluralities of sealant is adjoining on a side wall of said plurality of spacer walls; and

a transparent substrate is placed on said pluralities of said spacer walls.

2.The structure for a wafer level packaging according to claim 1, wherein a material of said pluralities of spacer walls is a silicon oxide compound.

3. The structure for a wafer level packaging according to claim 1, wherein a material of said pluralities of spacer walls is a silicon nitride compound.

4. The structure for a wafer level packaging according to claim 1, wherein a material of said pluralities of spacer walls is a polymer film.

5. The structure for a wafer level packaging according to claim 4, wherein said polymer film comprises a polyimide compound.

6. The structure for a wafer level packaging according to claim 1, wherein said

transparent substrate is a glass.

7. The structure for a wafer level packaging according to claim 1, wherein a material of said sealant is an epoxy adhesive.

8. The structure for a wafer level packaging according to claim 1, wherein a material of said sealant is an UV adhesive.

9. The structure for a wafer level packaging according to claim 1, wherein a material of said sealant is a thermo-plastic adhesive.

10. The structure for a wafer level packaging according to claim 1, wherein said side wall is an inner side wall.

11. The structure for a wafer level packaging according to claim 1, wherein said side wall is a outer side wall.

12. The structure for a wafer level packaging according to claim 1, wherein said pluralities of spacer walls comprise two units at least.

13. The structure for a wafer level packaging according to claim 12, wherein said pluralities of spacer walls further comprise placing on the opposite sites of said pluralities of dies.

14. The structure for a wafer level packaging according to claim 12, wherein said pluralities of spacer walls further comprise placing on the adjacent sites of

said pluralities of dies.

15. The structure for a wafer level packaging according to claim 1, wherein said pluralities of spacer walls further comprise having pluralities of individual unit with an arm shape.

16. The structure for a wafer level packaging according to claim 1, wherein said pluralities of spacer walls further comprise having pluralities of continuous unit with an arm shape.

17. A method for a wafer level packaging, comprising:

providing a semiconductor wafer, wherein said semiconductor wafer comprises pluralities of dies thereon;

depositing a dielectric layer on said semiconductor wafer and said pluralities of dies are covered;

removing a portion of said dielectric layer in order to form pluralities of spacer walls on said pluralities of dies;

forming pluralities of sealant and adjoining on a side wall of said pluralities of spacer walls; and

covering a transparent substrate on said semiconductor wafer.

18. The method for a wafer level packaging according to claim 17, wherein each of said pluralities of dies comprises a photosensitive zone.

19. The method for a wafer level packaging according to claim 17, wherein a step for removing said dielectric layer comprises exposing a photosensitive

zone.

20. The method for a wafer level packaging according to claim 19, wherein said photosensitive zone further comprises surrounding by four of said pluralities of spacer walls.

21. The method for a wafer level packaging according to claim 17, wherein said side wall is an inner side wall.

22. The method for a wafer level packaging according to claim 17, wherein said side wall is a outer side wall.

23. The method for a wafer level packaging according to claim 17, wherein a material of said transparent substrate is quartz.

24. A method for a wafer level packaging, comprising:

providing a semiconductor wafer and a transparent substrate, wherein said semiconductor wafer comprises pluralities of dies thereon;

depositing a dielectric layer on said transparent substrate;

depositing a photoresist layer on said dielectric layer;

removing a portion of said photoresist layer in order to expose a portion of said dielectric layer;

removing a portion of said exposed dielectric layer, utilizing said photoresist layer as a mask in order to form pluralities of spacer walls on said transparent substrate;

forming pluralities of sealant and adjoining a side wall of said pluralities of spacer walls; and

covering said semiconductor wafer on said transparent substrate.

25. The method for a wafer level packaging according to claim 24, wherein a step for removing said portion of said exposed dielectric layer comprises utilizing said pluralities of dies of said semiconductor wafer as a referable pattern.

26. The method for a wafer level packaging according to claim 24, wherein said side wall is an inner side wall.

27. The method for a wafer level packaging according to claim 24, wherein said side wall is a outer side wall.

28. The method for a wafer level packaging according to claim 24, wherein each of said pluralities of dies comprises a photosensitive zone.